On page 36, line 10, after "registers" insert --173--.

On page 36, line 12, after "registers" insert --172--.

On page 36, line 15, after "register" insert --171--.

On page 38, line 23, after the **second** occurrence of "register" insert --171--.

On page 38, line 25, after "register" insert --173--.

On page 39, line 6, after "register" insert --173--.

On page 54, line 13, delete "70" and substitute --69--.

IN THE DRAWING:

Please add new Figure 16, attached hereto.

IN THE CLAIMS:

Kindly **amend** the following claims:

151. (Amended) A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

a register which stores a value which is representative of a delay time after which the memory device responds to a read request; and

a plurality of output drivers to output data after [in accordance with] the delay time transpires and synchronously with respect to the external clock signal.

153. (Amended) The memory device of claim ~~152~~ wherein the plurality of output drivers output data in response to a rising edge of the external [internal] clock signal.

157. (Amended) A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

at least one register to store a value which is representative of a delay time; and

wherein in response to a read request, the memory device outputs data after [in accordance with] the delay time transpires and synchronously with respect to the external clock signal.

161. (Amended) The memory device of claim ~~157~~ wherein the memory device, in response to a control register access [set register request], stores a value in the at least one register.

163. (Amended) A method of controlling [operating] a synchronous [semiconductor] memory device having at least one

memory section including a plurality of memory cells and a register for storing a value which is representative of a time delay after which the memory device responds to a read request, the method comprising:

issuing a read request to the memory device; and

receiving data from [wherein] the memory device, in response to the read request, wherein the memory device outputs the data after [on a bus in accordance with] the time delay transpires and synchronously with respect to an external clock signal.

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24 23

~~164~~. (Amended) The method of claim ~~163~~ further including issuing a control register access [set register request], wherein, in response to the control register access [set register request], the memory device stores the value in the register.

25 24

~~165~~. (Amended) The method of claim ~~164~~ wherein the control register access [set register request] and the value are provided to the memory device in a single request packet.

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27 23

~~167~~. (Amended) The method of claim ~~163~~ further including [the steps of]:

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initializing the register in the memory device by issuing a control register access [set register request] on the bus; and

providing the value which is representative of the time delay.

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168. (Amended) The method of claim 163 further including [the step of] identifying the memory device on the bus using a device identification code.

Kindly **ADD** the following claims:

-- 173. The synchronous memory device of claim 151 wherein the value is representative of a number of clock cycles of the external clock.

174. The memory device of claim 173 wherein the value which is representative of the delay time is stored in the register after power is applied to the device.

175. The memory device of claim 174 further including:

a delay locked loop, coupled to the clock receiver circuitry, to generate an internal clock signal using at least the external clock signal; and

wherein the plurality of output drivers output data in response to the internal clock signal.

176. The memory device of claim 174 wherein the value stored in the register is representative of one of a plurality of different delay times.

177. The synchronous memory device of claim 157 wherein the value is representative of a number of clock cycles of the external clock signal..

178. The memory device of claim 177 wherein the value which is representative of the delay time is stored in the register after power is applied to the device.

179. The memory device of claim 177 further including:

a delay locked loop, coupled to the clock receiver circuitry, to generate an internal clock signal using at least the external clock signal; and

wherein the plurality of output drivers output data in response to the internal clock signal.

180. The memory device of claim 177 wherein the memory device outputs data in response to a rising edge of the external clock signal.

181. The memory device of claim 180 further including:

clock generation circuitry, coupled to the clock receiver circuitry, to generate an internal clock signal; and

an output driver, coupled to the internal clock generation circuitry, to output the data in response to the internal clock signal.

182. The memory device of claim 181 wherein the output driver outputs data in response to a rising edge of the internal clock signal.

183. The method of claim 163 wherein the external clock signal has a fixed frequency.

184. A synchronous semiconductor memory device having at least one memory section including a plurality of memory cells, the memory device comprising:

clock receiver circuitry to receive an external clock signal;

a register which stores a value which is representative of a number of cycles of the external clock signal to transpire after which the memory device responds to receiving a request to provide data; and

a plurality of output drivers to output data in response to receiving a request to provide data, wherein the data is provided after the number of cycles of the external clock signal represented by the value have transpired.

185. The memory device of claim 184 wherein the plurality of output drivers output data synchronously with respect to a transition of the external clock signal.

186. The memory device of claim 184 further including input receiver circuitry, coupled to the bus, to receive the request to provide data, wherein the request to provide data is sampled from the bus synchronously with respect to the external clock signal.

187. The memory device of claim 186 wherein the input receiver circuitry further includes a first input latch coupled to the bus, wherein the first input latch samples a first information bit synchronously with respect to a rising edge of the external clock signal.

188. The memory device of claim 187 wherein the input receiver circuitry further includes a second input latch coupled to the bus, wherein the second input latch samples a second information bit synchronously with respect to a falling edge of the external clock signal.

189. The memory system of claim 188 the first and second information bits are included in the request to provide data, and